What is claimed are:

1. A method of forming an isolation film in a semiconductor device, comprising:

forming a stack structure of a pad oxide film and a photoresist which an isolation region is defined pattern on a semiconductor substrate, the isolation region having one or more corners and a central portion, the photresist pattern containing silicon;

implementing an over etch so that polymer is formed at the corners of the isolation region to form an etch slant face at one or more corners of the isolation region while etching the semiconductor substrate at the central portion of the isolation region;

forming a trench at the central portion of the isolation region;

oxidizing a surface of the photoresist pattern to form a surface oxide film;

forming an insulating material layer on the entire structure to bury the trench; and

implementing a polishing process until the photoresist pattern has a given thickness and then removing the photoresist pattern and the pad oxide film.

2. The method as claimed in claim 1, wherein the amount of silicon contained in the photoresist pattern is in the range of from about 7 to about 50%.

3. The method as claimed in claim 1, wherein the over etch process uses a CHF_3 gas, a CF_4 gas or a mixture thereof as an etch gas to etch the central portion of the isolation region in depth an amount ranging from about 50 to about 400 Å.

4. The method as claimed in claim 3, wherein a supply flow of CHF_3 is from about 50 to about 70 sccm, the supply flow of CF_4 is from about 30 to about 50 sccm and an Ar gas flow of from about 1000 to about 2000 sccm is supplied as a carrier gas.

5. The method as claimed in claim 1, wherein the over etch process is implemented for a time period from about 5 to about 30 seconds with a pressure of from about 500 to about 2500 mTorr and a power of from about 600 to about 2000 W is applied.

6. The method as claimed in claim 1, wherein a width of the etch slant face is from about 0.02 μm to about 0.07 μm and a tilt angle of the sidewall of the etch slant face is from about 20 to about 50°.

7. The method as claimed in claim 1, wherein the surface oxide film is formed by means of an O_2 plasma processing.

8. The method as claimed in claim 7, wherein the O_2 plasma processing is implemented at a temperature ranging from about 50 to about 200 °C by means of an O_2 ashing process or an O_2 ion implantation process.

9. The method as claimed in claim 1, wherein the insulating material layer is formed using a low thermal oxide film at a temperature ranging from about 50 to about 300 °C.

10. A method of forming an isolation film in a semiconductor device, comprising the steps of:

forming a stack structure of a pad oxide film, an amorphous silicon layer, an anti-reflection film and a photoresist pattern on a semiconductor substrate which an isolation region is defined;

implementing an over etch so that polymer is formed at a corner of the isolation region to form an etch slant face at the corner of the isolation region while etching the semiconductor substrate at the central portion of the isolation region;

removing the photoresist pattern and the anti-reflection film;

oxidizing the surface of the amorphous silicon layer to form a surface oxide film;

forming an insulating material layer on the entire structure to bury a trench; and

implementing a polishing process until the insulating material layer is at a given thickness and then removing the amorphous silicon layer and the pad oxide film.

11. The method as claimed in claim 10, wherein the over etch process uses a CHF_3 gas, a CF_4 gas or a mixed gas of them as an etch gas to etch a central portion of the isolation region in depth in an amount ranging from about 50 to about 400 Å.

12. The method as claimed in claim 10, wherein the width of the etch slant face ranges from about 0.02μm to about 0.07μm and a tilt angle of the sidewall of the etch slant face ranges from about from 20 to about 50°.

13. The method as claimed in claim 10, further comprising the step of before the surface of the amorphous silicon layer is oxidized after the anti-reflection film is removed, oxidizing the sidewall and bottom of the trench to form a surface oxide film at the sidewall and bottom of the trench.

14. The method as claimed in claim 10, wherein the surface oxide film is formed by means of an O_2 plasma processing.

15. The method as claimed in claim 14, wherein the O_2 plasma processing is implemented at a temperature ranging from about 50 to about 200°C by means of an O_2 ashing process or an O_2 ion implantation process.

16. A method of forming an isolation film in a semiconductor device, comprising the steps of:

stacking a pad oxide film, an amorphous silicon layer, an anti-reflection film and a photoresist pattern on a semiconductor substrate which an isolation region is defines;

implementing over etch so that polymer is formed at a corner of the isolation region to form an etch slant face at the corner of the isolation region while etching the semiconductor substrate at the central portion of the isolation region;

etching a part of the semiconductor substrate using the polymer film as an etch mask to form a trench;

burying the trench with an insulating film and then removing the polymer film and a hard mask film;

implementing an O_2 plasma oxidization process to oxidizing the amorphous

silicon film on the amorphous silicon film and at the sidewall of the insulating film, thus forming an oxide film;

etching the oxide film on the amorphous silicon film; and

etching the amorphous silicon film and the pad oxide film below the amorphous silicon film.

17. The method as claimed in claim 16, wherein the O_2 plasma oxidization process is implemented to oxidize a top and sidewall of the amorphous silicon film using a plasma ashing method and an O_2 ion implantation method having a temperature ranging from about 50 to about 200°C.

18. The method as claimed in claim 16, wherein the polymer film is formed by etching about 200Å of the semiconductor substrate using a gas such as CF_4 and CHF_3.